AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system for detecting transaction errors in a system comprising a plurality of data processing devices using a common system interconnect bus, comprising:

a node controller operably ~~connected~~ coupled to said system interconnect bus;

a plurality of interface agents communicatively coupled to said node controller;

an address table comprising a plurality of predetermined addresses corresponding to predetermined transaction error conditions;

wherein errors corresponding to transactions between said interface agents and other processing modules in said system are directed to said node controller; and

wherein ~~transaction errors that would not normally be communicated to said system interconnect bus are communicated by said node controller~~ said node controller is operable to flag said errors using said predetermined addresses and to communicate said errors to said system interconnect bus ~~to be available~~ for detection.

2. (Original) The system of claim 1, wherein said interface agents operate in accordance with the hypertransport protocol.

3. (Currently Amended) The system of claim 1, ~~futher~~ further comprising a system control and debug module operably connected to said system interconnect bus[[;]].

4. (Currently Amended) The system of claim 3, further comprising a trace cache operably connected to said system control and debug module, wherein said errors are detected by said trace cache and said system control and debug module.

5. (Original) The system of claim 1, wherein said node controller sends said transactions corresponding to said errors to predetermined register addresses corresponding to error conditions.

6. (Original) The system of claim 5, wherein said transactions corresponding to said errors comprise input/output transactions.

7. (Original) The system of claim 5, wherein said transactions corresponding to said errors comprise control commands.

8. (Original) The system of claim 5, wherein said transactions corresponding to said errors comprise a writes to memory addresses.

9. (Original) The system of claim 5, wherein said transactions corresponding to said errors comprise reads from memory addresses.

10. (Original) The system of claim 5, wherein said errors communicated to said system interconnect bus are stored in said trace cache.

11. (Original) The system of claim 9, wherein in said trace cache is programmable to store only a predetermined set of errors corresponding to a specified diagnostic protocol.

12. (Currently Amended) A method for detecting transaction errors in a system comprising a plurality of data processing devices using a common system interconnect bus, comprising:

detecting an error corresponding to a transaction between an interface agent and another processing module in said system~~, wherein said transaction error would not normally be communicated to said system interconnect bus~~;

flagging said error using a predetermined address in an address table, said predetermined address corresponding to a predetermined transaction error condition; and

communicating said transaction error to said system interconnect bus ~~whereby said error is available~~ for detection by a plurality of system modules ~~connected~~ coupled to said system interconnect bus.

13. (Original) The method of claim 12, wherein

said interface agent in operably connected to a switch;

said switch is operable connected to a node controller; and

said node controller is operably connected to said system interconnect bus.

14. (Original) The method of claim 13, wherein said interface agent operates in accordance with the hypertransport protocol.

15. (Original) The method of claim 13, , wherein said node controller writes said transactions corresponding to said errors to predetermined register addresses corresponding to error conditions.

16. (Original) The method of claim 15, wherein said transactions corresponding to said errors comprise input/output transactions.

17. (Original) The method of claim 15, wherein said transactions corresponding to said errors comprise control commands.

18. (Original) The method of claim 15, wherein said transactions corresponding to said errors comprise a writes to memory addresses.

19. (Original) The method of claim 15, wherein said transactions corresponding to said errors comprise reads from memory addresses.

20. (Original) The method of claim 15, wherein said errors communicated to said system interconnect bus are stored in a trace cache.